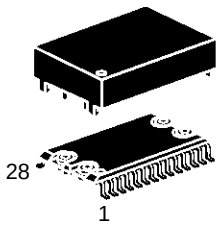
SGS-THOMSON MICROELECTRONICS

M48T558

ADDRESS/DATA MULTIPLEXED 8K x 8 TIMEKEEPER SRAM

PRODUCT PREVIEW

- REGISTER COMPATIBLE with M48T58 and M48T18 TIMEKEEPER SRAM
- ADDREES/DATA MULTIPLEXED I/O PINS
- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT and BATTERY
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- FREQUENCY TEST OUTPUT for REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGE:
  - M48T558Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE



SOH28 (MH)
Battery SNAPHAT

DESCRIPTION

The M48T558 TIMEKEEPER™ RAM is an 8K x 8 non-volatile static RAM and real time clock. The monolithic chip is available in the SNAPHAT package to provide a highly integrated battery backed-up memory and real time clock solution.

Table 1. Signal Names

AD0-AD7	Address/Data
$\overline{AS0}$, $\overline{AS1}$	Address Strobes
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{E}$	Chip Enable
FT	Frequency Test Output (Open Drain)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

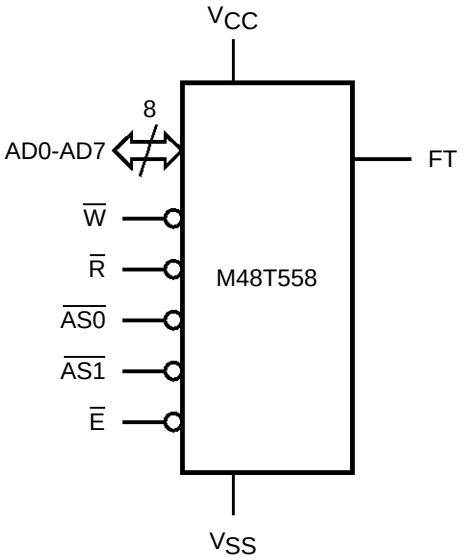
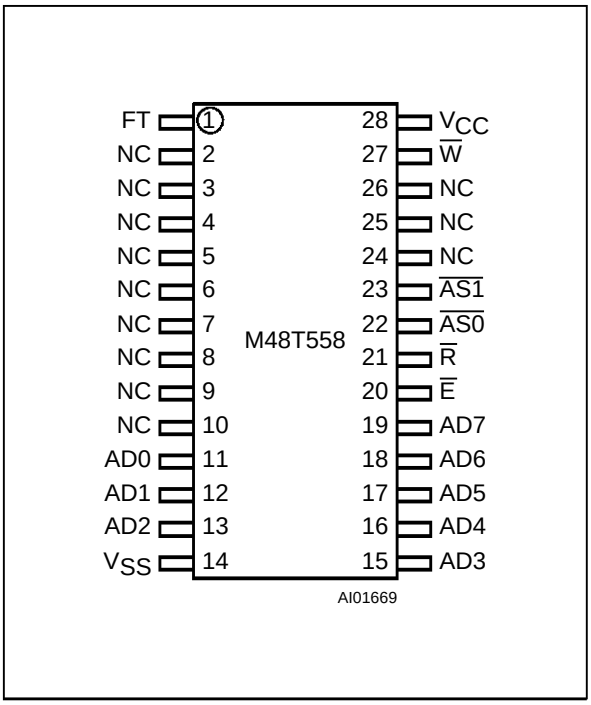


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Figure 2. SO Pin Connections



Warning: NC = Not Connected.

DESCRIPTION (cont'd)

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T558 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T558 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

Figure 3. Block Diagram

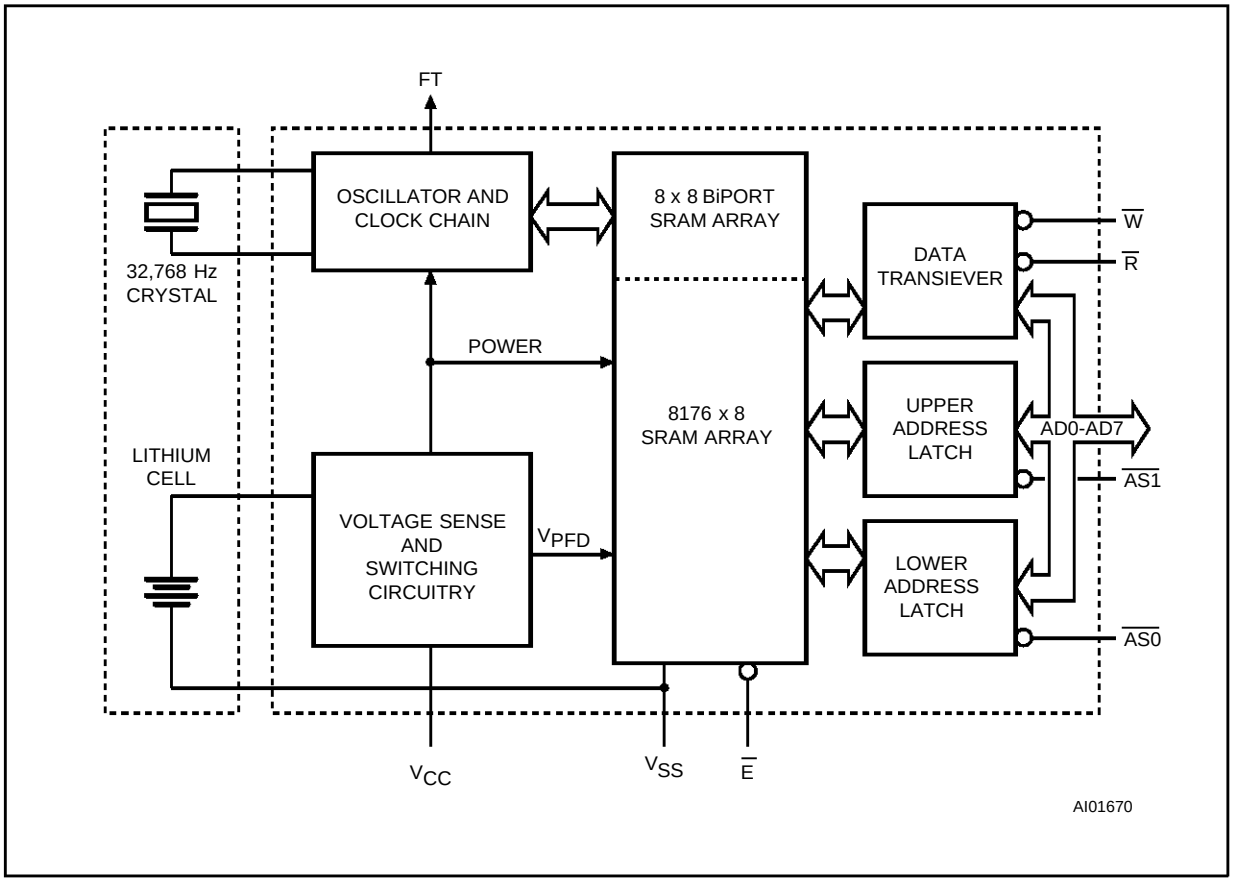


Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{R}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details..

The M48T558 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

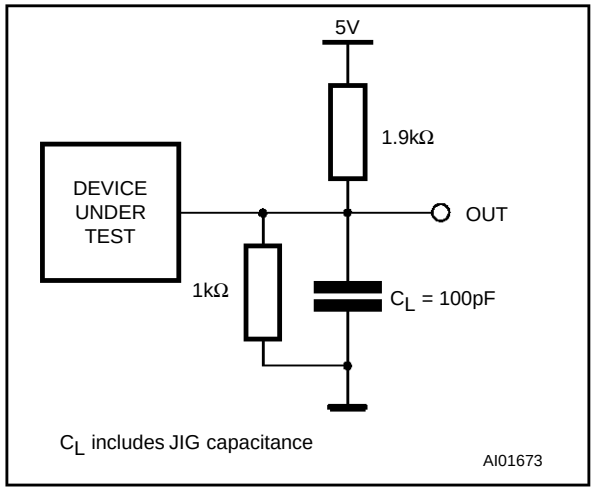


Table 4. Capacitance (1, 2) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (3)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL} (2)	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage (FT) (3)	I_{OL} = 10mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Negative spikes of –1V allowed for up to 10ns once per cycle.
3. The FT pin is Open Drain.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T558Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	7			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD} (max) to Inputs Recognized	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

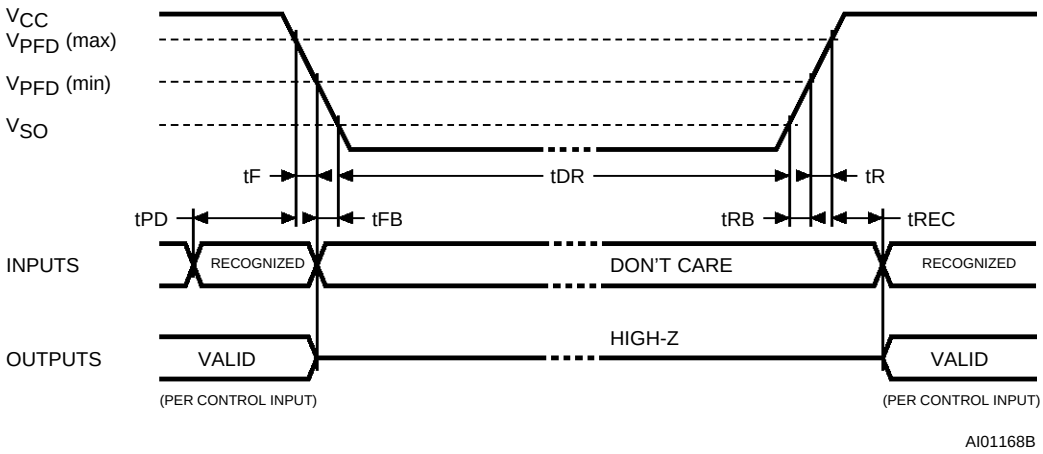
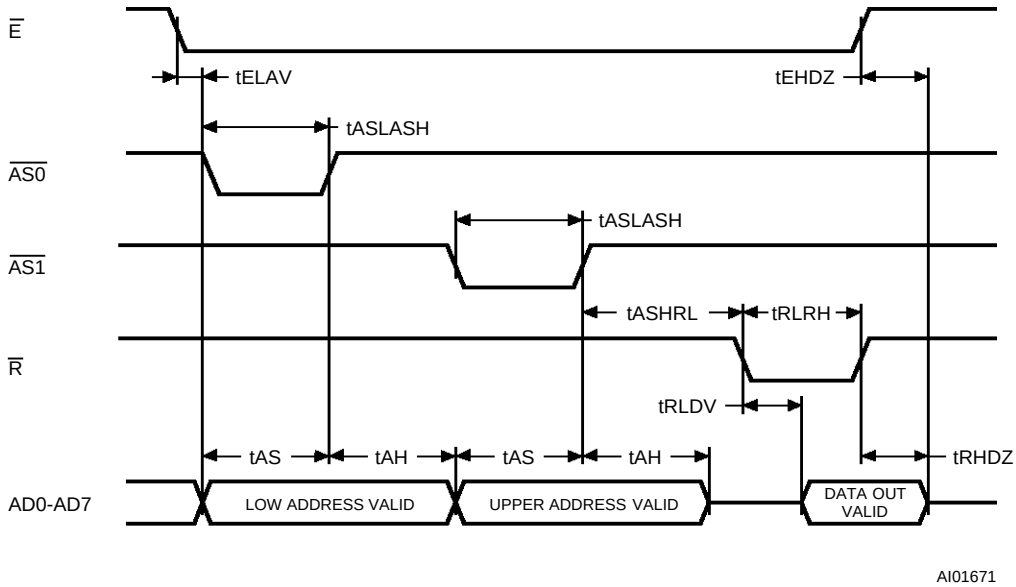
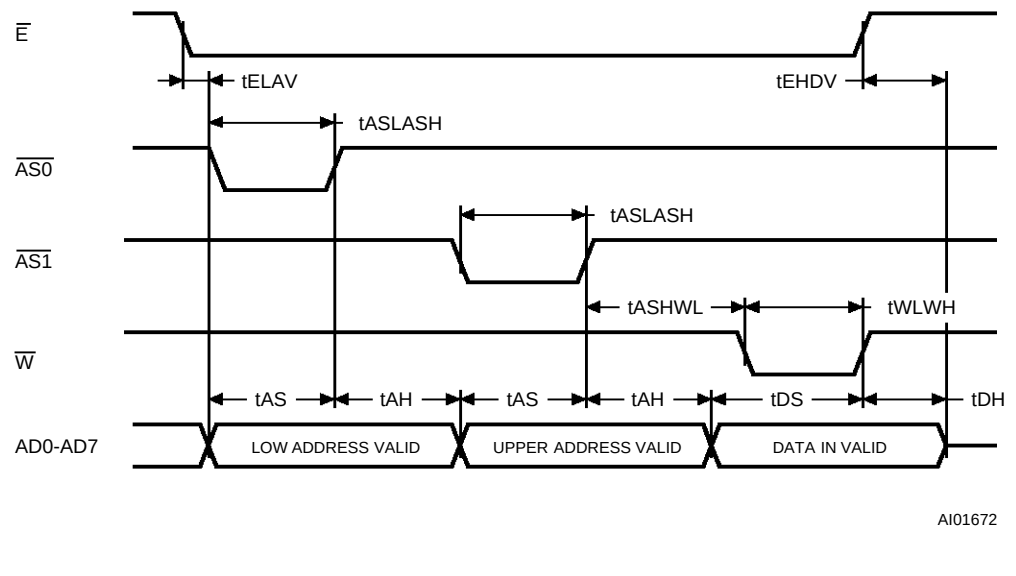


Figure 6. Read Mode AC Waveforms



Note: AD5-AD7 are don't care when latching upper address.

Figure 7. Write Mode AC Waveforms



Note: AD5-AD7 are don't care when latching upper address.

Table 8. AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	M48T558Y		Unit
		Min	Max	
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	0		ns
t_{DS}	Data Setup Time	60		ns
t_{DH}	Data Hold Time	0		ns
t_{RLDV}	Read Enable Access Time		70	ns
t_{RLRH}	$\overline{R}$ Pulse Width Low	70		ns
t_{RHDZ}	Read Enable High to Output High Z		25	ns
t_{WLWH}	$\overline{W}$ Pulse Width Low	50		ns
t_{ASLASH}	$\overline{AS0}$, $\overline{AS1}$ Pulse Width Low	15		ns
t_{ASHRL}	$\overline{AS0}$, $\overline{AS1}$ High to $\overline{R}$ Low	15		ns
t_{ASHWL}	$\overline{AS0}$, $\overline{AS1}$ High to $\overline{W}$ Low	15		ns
t_{ELAV}	Chip Enable Low to Address Valid			ns
t_{EHDZ}	CHip Enable High to Data Output Hi-Z			ns
t_{EHDV}	Chip Enable High to Data Valid			ns

RAM OPERATION

Four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{R}$ and $\overline{W}$, are used to access the M48T558. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 ($\overline{AS1}$) signals. $\overline{AS0}$ is used to latch the lower 8 bits of address, and $\overline{AS1}$ is used to latch the upper 5 bits of address. It is necessary to meet the set-up and hold times given in the AC specifications with valid address information in order to properly latch the address. If the upper and/or lower order addresses are correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation reqires valid data to be placed on the bus (AD0-AD7) followed by the activation of the Write Enable ($\overline{W}$) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Read Enable ($\overline{R}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met.

The $\overline{W}$ and $\overline{R}$ signals should never be active at the same time. In addition $\overline{E}$ must be active before any control line are recognized.

DATA RETENTION MODE

With valid V_{CC} applied, the M48T558 supports industry standard read and write operations. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T558 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T558 for an accumulated period of at least 7 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Deselect continues for t_{REC} after V_{CC} reaches V_{PFD}(max).

Table 9. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFh	10 Years				Year				Year	00-99
1FFEh	0	0	0	10 M.	Month				Month	01-12
1FFDh	0	0	10 Date		Date				Date	01-31
1FFCh	0	FT	0	0	0	Day			Day	01-07
1FFBh	0	0	10 Hours		Hours				Hour	00-23
1FFAh	0	10 Minutes			Minutes				Minutes	00-59
1FF9h	ST	10 Seconds			Seconds				Seconds	00-59
1FF8h	W	R	S	Calibration					Control	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit (Must be set to '0' upon power, for normal clock operation)
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, D6 in the Control register (1FF8h). As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

Bit D7 of the Control register (1FF8h) is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 9). Resetting the WRITE bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 9 must be written to '0' to allow for normal TIMEKEEPER and RAM operation. After the WRITE bit is reset, the next clock update will occur in one second.

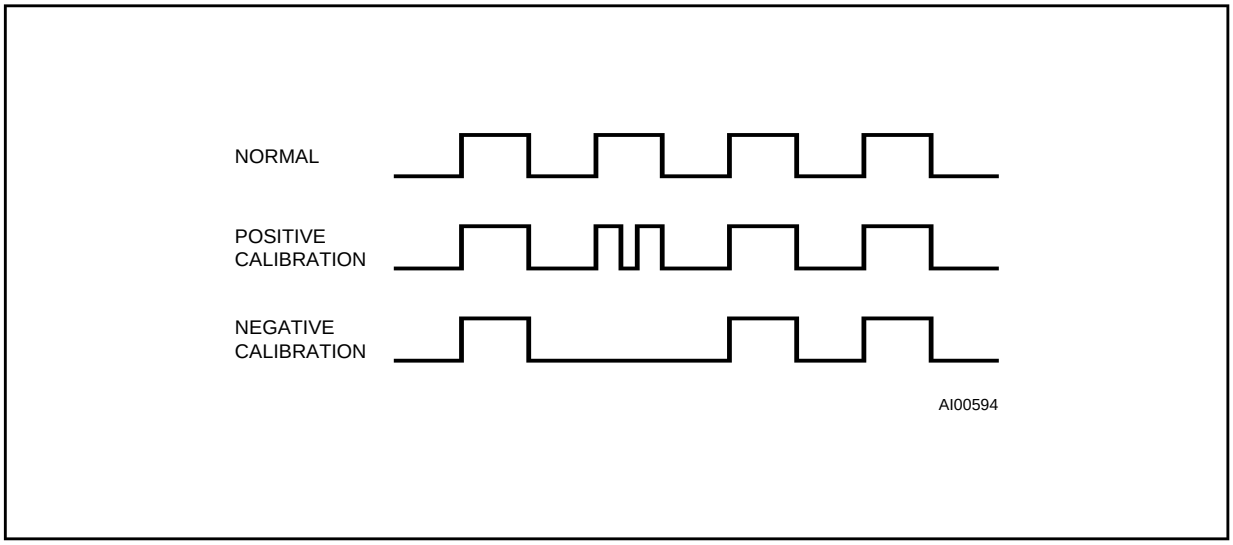
Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T558 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T558 oscillator starts within 1 second.

Calibrating the Clock

The M48T558 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T558 improves to better than ±4 PPM at 25°C.

Figure 9. Clock Calibration



Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T558 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 9. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five Calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits (D4-D0) in the Control register (1FF8h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

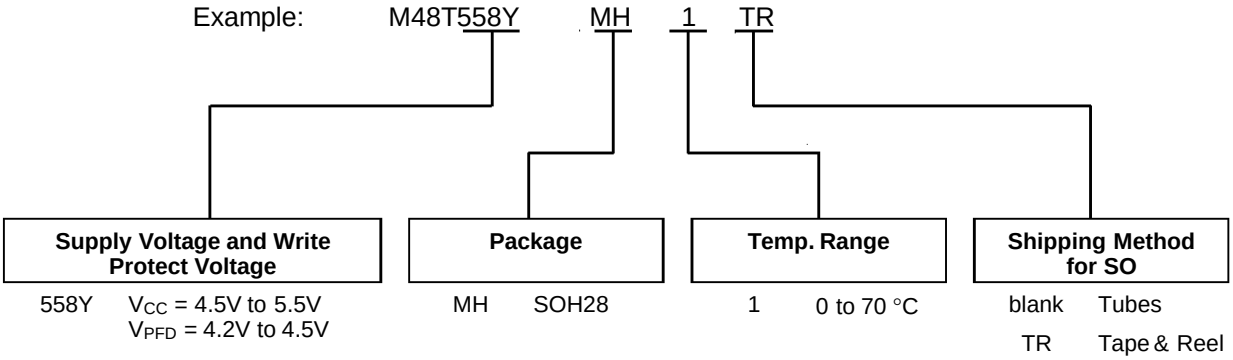
Two methods are available for ascertaining how much calibration a given M48T558 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a '1', and the oscillator is running at 32,768 Hz, the Frequency Test (Pin 1) will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

The FT bit must be set using the same method used to set the clock, using the Write bit.

The Frequency Test pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10kΩ resistor is recommended in order to control the rise time.

ORDERING INFORMATION SCHEME



The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

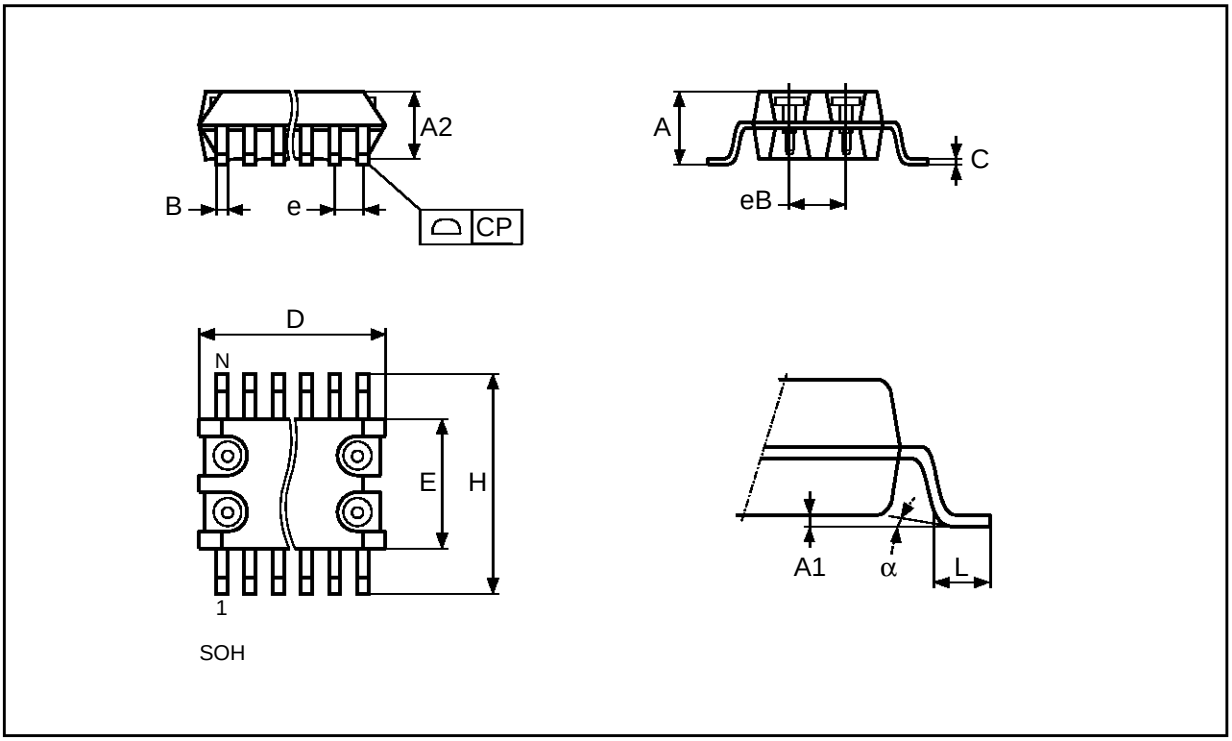
For a list of available options (Supply Voltage, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28



SOH

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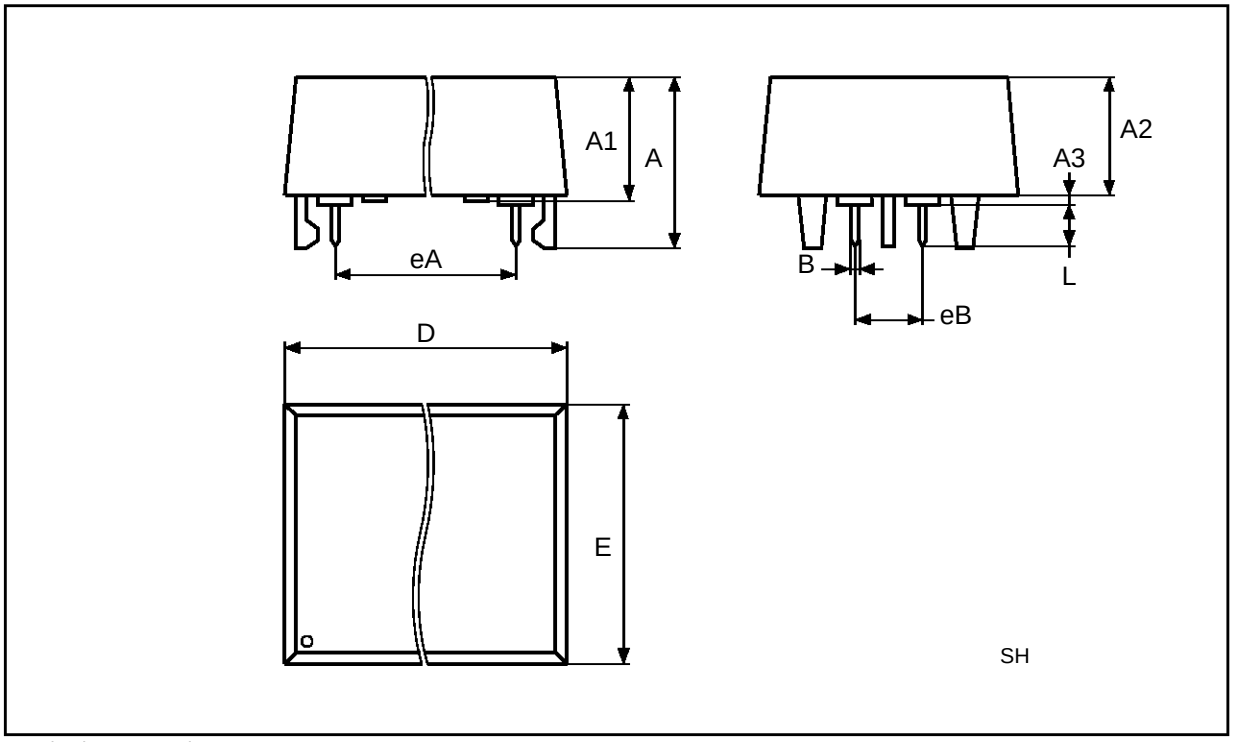
SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28



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